## REMARKS/ARGUMENTS

Claims 1 and 12 have been amended, claims 2 – 6 and 13 – 16, have been canceled, and claims 8 and 9 have been amended to refer to claim 1 rather than to canceled claim 2.

In the office action, claims 1-10, and 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimura et al. (US 6,806,428). Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Okabe et al. (US 6,757,178).

It is noted that, the fabrication of the structure of Kimura et al. comprises forming conductive connections on copper foils 32 formed on the top surface and the bottom surface of a substrate 31 before forming a plurality of penetration holes 35 for placing passive chips 36 and 37, wherein the copper foils 32 are proceeded by the patterning process to form a circuit wiring pattern 34 before placing the passive chips 36 and 37 into the penetration holes 35; applying conductive resins at electrodes 36a and 37a formed on the top surface and the bottom surface of the passive chips 36 and 37 to form connection electrodes 38, as shown in FIG. 6(g); forming auxiliary substrates 39 and copper foils 40 on the connection electrodes 38; and then forming surface circuit wiring patterns 43 by the etching process.

Accordingly, Kimura et al. suggests that the wiring pattern should be formed first by the copper foil 32 formed on the surface of the substrate 31 before placing the passive chips 36 and 37 into the holes in the substrate. On the contrary, the present invention suggests that the substrate is first formed with penetration openings before inserting passive materials into the openings, and then a conductive layer is formed on the surfaces of the passive material and the substrate. After that, the conductive layer is then used to form a wiring pattern according to the requirement.

Seemingly, the steps of the fabrication methods disclosed by Kimura et al. and the present invention are proceeded in different order. Therefore, Kimura et al. is still not convincing enough to prove that the present invention is not novel.

Additionally, as the passive materials (capacitive materials) disclosed in the present invention are first inserted into the core layer before forming the conductive layer, the more complicated processes such as inserting the passive chips into the holes of the substrate after the formation of connection electrode electrically connected to the circuit wiling pattern are thereby eliminated. As aforementioned, the fabrication disclosed by the present invention is much simpler, therefore Kimura et al. fails to prove that the present invention is not novel.

Further, the passive components disclosed in Kimura et al. are chips, wherein the top and the bottom of passive components comprise electrode pads; however, the present invention employs only the capacitive materials, thus these two passive components are constructed distinctively. Furthermore, the present invention suggests forming a conductive layer as a whole on the core layer and the capacitive materials and then patterning the conductive layer to form conductive traces so as to electrically connect the circuit layer to the capacitive materials. Besides, claims 1 and 12, after amended, confine that the conductive traces are partly used as parallel sheets of embedded capacitive materials, and therefore it is distinguished over Kimura et al. forming the circuit wirings on the substrate and employing the connection electrodes 38 formed by the conductive resin to electrically connect the passive chip, circuit wiring pattern 34 and surface circuit wiring pattern 43. However, the present invention does not employ the conductive resin to form the connection electrodes 38, thereby the final structure of the product is different from Kimura et al. Accordingly, Kimura et al. does not teach or suggest forming a simpler structure as disclosed in the present invention, therefore fails to prove that the present invention is obvious and not novel.

The Applicant wishes to emphasize once again that the characteristic feature of the present invention is that after forming the openings on the core layer, the capacitive materials are filled thereto directly. In addition, the value of the capacitance is determined by the size of the openings that will be filled with the capacitive materials of the present invention. Therefore the size of the openings may be changed according to the requirement so as to alter the value of the capacitance. Moreover, the value of the capacitance may be defined according to the circuit needs, which are formed with electrical connection between the capacitors

by the patterned conductive traces. Accordingly, the present invention has greater flexibility and choices for improving the functions and performances and thereby does hold an inventive step. In fact, none of the references (Kimura et al.; Okabe et al.) nor the combination of Kimura et al. in view of Okabe et al. suggest or teach such foregoing, therefore the present invention is proved to be non obvious.

The Applicant respectfully disagrees with the Examiner's opinion. The Applicant believes that the present invention is clearly defined in the independent claims. However, to make the present invention distinguished over the cited references, the Applicant proceeds with the amendment as enclosed herewith.

In summary, it is submitted that independent claims 1 and 12, amended, are patentable. Inasmuch as claims 1 and 12 are believed to be patentable, the dependent claims, which depend therefrom, are likewise believed to be patentable.

Accordingly, a Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge payment of any fees required associated with this communication or credit any overpayment to Deposit Account No. 50-0337. If an extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. 50-0337. A duplicate copy of this paper is enclosed.

Respectfully submitted,

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